KOCAELI UNIVERSITY, DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

RESEARCH PROJECT

Analog Circuit Design Automation for Sense and React Systems

Opening Position: Undergraduate/Graduate Researcher

Engin AFACAN, PhD

August 29, 2018

This project is supported by the research grant of the Kocaeli University Council of Scientific Research Project (BAP) under the project number 2018/084.

1 PROJECT DESCRIPTION

Thanks to rapid developments in CMOS technology, it has been possible to design high performing integrated circuits, which consume less power and occupy smaller chip area. In addition to these improvements, CMOS integrated circuits have been affected by worsening process variations and severe time dependent degradation mechanisms (aging); hence, reliability has become one of major design objectives as well as electrical design objectives. In the literature, a number of different approaches have been proposed to analyze both variability and aging problems. Reliability analyses performed during/after design process aim to estimate the performance of integrated circuits both after the production and a certain operation period, investigate ad-hoc design techniques to mitigate performance loss, and finally re-evaluate the design. The well-known technique to increase the yield of manufactured ICs and lifetime of circuits is designing re-configurable integrated circuits. In this approach, circuits are re-configured according to a pre-determined recovery scenario when performance of them degrades below to intended specifications. Sense and React is the well-known re-configurable circuit design approach. In this approach, performance of ICs is monitored either continuously or discontinuously, performance losses are sensed via ad-hoc sensor circuitry, and a pre-determined recovery scenario are switched on. The most valuable advantage of this technique is perfect recovery of circuit without any performance loss. Another important advantage is that this approach enables online and remote monitoring of degradation, where recovery operation is also remotely applied in any urgent case. Furthermore, chip area does not excessively increase since most of the peripheral circuits are digital. At last, there would not be any additional power consumption if the system is designed as working discontinuously. After all these advantages, the only drawback of this approach is design complexity. Online measuring of performance losses in the chip and determination and design of recovery operation are difficult problems all on them own, where all individual circuit requires specific solution. As a result, design time excessively increases compared to a conventional analog design problem. Utilizing CAD tools may facilitate the design process and reduce the design time; however, any fully automatic design tool has not been developed in the literature, where most of studies have focused on specific applications and proposed specific solutions for these applications. In summary, a designer should manually design the system from sensor circuitry to recovery operation including all the intermediate steps (signature selection, evaluation, etc.). Considering all of these complicated design problems, design automation tool for sense and react systems is required to reduce the design time and minimize the design cost. In this project, development of a design automation tool for reconfigurable CMOS analog circuits is aimed. The developed tool will be used in design of sense and react systems for all analog ICs without any topology dependency; thus, design time and the cost of design will be considerably reduced.

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2 Required Skills

- Demonstrated verbal and written ability to communicate effectively.
- Ability to establish and maintain effective working relationships.
- High degree of analytical problem solving skills and the ability to connect the dots to make reliable, objective judgments and proposals.
- Excellent written and verbal communication skills both in English and Turkish.
- Excellent time planning and multi-tasking skills.
- A solid knowledge on analog/RF circuit design, simulation, and verification.
- Knowledge on SPICE and Matlab/Phyton/C.

3 RESEARCH DUTIES

- A comprehensive literature search.
- Re-configuration of the aging simulator.
- Development of the signature selection automation tool.
- Development of an IP for Sense operation.
- Automation of the recovery operation.
- Accomplishment of the design automation loop.

4 Important Details

- The project duration is 18 months, which has already started on 07.04.2018 (Therefore, direct action is required).
- The gross salary per month for this position is 1000TL (pre-tax, 8 times), which is the default salary as defined by the BAP.
- Please personally contact to Assist. Prof. Dr. Engin Afacan (engin.afacan@gmail.com) no later than the 23th of September, 2018.

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