Course Syllabus

MEH-219 -2015-2016 1st Semester

DIGITAL DESIGN (A/B)
Monday 10:00-11:50 / Thursday 09:00-10:50

Instructors:
Dr. Mehmet Yakut 1020, Engineering Building B (262)303-3367, myakut@kocaeli.edu.tr
Dr. Anıl Çelebi 1008, Engineering Building B (262)303-3354, anilcelebi@kocaeli.edu.tr

Office Hours (Mehmet Yakut): TBA
Office Hours (Anıl Çelebi): TBA


Reference Books:

Course Prerequisites: None

Schedule:

1. Overview of the course: topics covered, mark assignments (midterm test, labs, final exam), quick overview of digital systems and Moore's law, examples of digital systems, overview of how the lab exercises are organized (students work in small groups (two per group?), marks assigned for preparation and lab performance); short introduction to the DE2 board (its FPGA can be used to implement any digital circuit that fits in this chip, it has lots of useful I/O features). Reading: Brown Ch.1 (20)

2. Cont’d

3. Transistors as simple on-off switches; introduction to logic expressions; AND, OR, NOT circuits built using switches; AND, OR, NOT gate symbols; truth tables; simple example of logic circuit with AND, OR, NOT gates. Reading: Brown Ch B.1(3), 2.1-2.4(12)

4. Boolean algebra: duality, axioms, rules, identities; proof of identities using perfect induction (i.e., truth tables); algebraic manipulation of Boolean expressions; timing diagrams; Venn Diagrams and their use to prove some identities. Reading: Brown Ch. 2.5(11)

5. Boolean Algebra cont’d. Reading: Brown Ch. 2.5(11)

6. Simple synthesis of logic circuits; sum-of-products (SOP) form; minterms; canonical SOP; product-of-sums form (POS); maxterms; canonical POS; examples of algebraic manipulation. Reading Brown: Ch 2.6(12)

7. Cont’d; Example logic functions: 2-to-1 multiplexer, XOR gate; NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-NOR. Reading: Brown Ch. 2.7-2.8(11)

8. Cont’d

9. Binary numbers; full adder, ripple-carry adder. Reading: Brown Ch 3.1-3.2(11)

10. Cont’d; Introduction to CAD tools; introduction to VHDL/Verilog. Reading: Brown Ch. 2.9-2.10(14)
11. Cont’d
12. Introduction to Field Programmable Gate Arrays (FPGAs). **Reading: Brown B.6(14)**
13. Introduction to cost of a logic circuit; terminology: implicant, prime implicant (PI), essential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables). **Reading: Brown Ch 2.11-2.13(17)**
14. Cont’d;
15. 5-variable K-maps; don't cares, and examples; 7-seg example. **Reading: Brown Ch. 2.11-2.15(24, Lab1, Lab2)**
16. Cont’d
17. Review
18. Quiz I
19. Storage elements: introduction, RS latches, timing diagrams, gated RS latch. **Reading: Brown Ch. 5.1 - 5.2(15)**
20. Cont’d
21. Gated D latch, D flip-flops, setup and hold times. **Reading: Brown Ch 5.3-5.4(11)**
22. Cont’d; Flip-flop reset/preset; registers; shift registers; parallel load. **Reading: Brown Ch. 5.4-5.8(14)**
23. Cont’d
24. Counters; ripple and synchronous counters. **Reading: Brown Ch 5.9-5.11(16)**
25. Cont’d
26. VHDL/Verilog code for synchronous circuits, Timing analysis of logic circuits. **Reading: Brown Ch. 5.12 - 5.15(26, Lab3, Lab4, Lab5)**
27. Cont’d
28. Cont’d
29. Signed numbers; 2's complement; adders/subtractors. **Reading: Brown Ch 3.3(14)**
30. Cont’d
31. Design of arithmetic circuits using CAD tools, Multipliers. **Reading: Brown Ch. 3.5-3.6(20)**
32. Cont’d
33. Cont’d
34. Midterm
35. Midterm
36. Midterm
37. Midterm
38. Midterm
39. Midterm
40. Midterm
41. Midterm
42. Combinational circuits: implementing logic functions using only multiplexers. **Reading: Brown Ch 4.1-4.3(19)**
43. Cont’d
44. Decoders, encoders, code converters, comparators; VHDL/Verilog. **Reading: Brown Ch. 4.2-4.6(25, Lab6)**
45. Cont’d
46. Cont’d
47. Review
49. Cont’d
50. FSMs: State Assignment, Mealy Model. **Reading: Brown Ch. 6.2-6.3(10)**
51. FSMs: Design of FSM Using CAD Tools; Verilog/VHDL code. **Reading: Brown Ch 6.1-6.5(19, Lab 7)**

52. **Cont’d**

53. **Cont’d:** FSMs: State Minimization. **Reading: Brown Ch. 6.6(12)**

54. FSMs: Arbiter Example, **Reading: Brown Ch. 6.8, 6.10-6.12(10)**

55. **Cont’d:** Memory: Introduction to SRAM. **Reading: Brown Ch B.9(4)**

56. Quiz II

57. Memory: SRAM blocks in an FPGA. **Reading: Brown Ch. B.9-B.10(13)**


59. Digital System Design: Simple Processor. **Reading: Brown Ch. 7.2(12)**

60. **Cont’d:** Examples: Bit Counting Circuit, Shift and Add Multiplier **Reading: Brown Ch. 7.3-7.4(13)**

61. **Cont’d.**

62. Review

63. Transistor circuits; building logic gates with transistors; CMOS. **Reading: Brown Ch. B.1-B.3(6)**

64. Speed of transistor circuits: propagation delay, rise/fall time, fanout. **Okuma: Brown Ch B.1 - B.3(6)**

Lab 9 and Lab 10 is optional for getting extra points.

**Grading Policy:**

<table>
<thead>
<tr>
<th>Course Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>1 Midterm Exam</td>
<td>50%</td>
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<tr>
<td>2 Quizes</td>
<td>20%</td>
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<tr>
<td>7 Labs</td>
<td>30%</td>
</tr>
<tr>
<td>1 Final Exam</td>
<td>40%</td>
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**60%**

**Lab Tools:**

- **Altera Platform**
  - Tutorials: [https://www.altera.com/support/training/university/materials-tutorials.tablet.highResolutionDisplay.html](https://www.altera.com/support/training/university/materials-tutorials.tablet.highResolutionDisplay.html)

- **Xilinx Platform**
  - Zybo Board: [http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1198&Prod=ZYBO](http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1198&Prod=ZYBO)
  - Nexsys4DDR Board: [http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1338&Prod=NEXYS4DDR](http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1338&Prod=NEXYS4DDR)